
DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to semiconductor memories, such as a ferroelectric RAM which has the capacitor which used the ferroelectric as a dielectric film.
[0002]
[Description of the Prior Art] When electric field are impressed, the once generated electric polarization remains, even if this electric field are no longer impressed, and with said electric field, the ferroelectric film has the property which the sense of polarization reverses, when the electric field of the strength of a more than are impressed to some extent to the sense of an opposite direction. Paying attention to the polarization property which the sense of polarization of this ferroelectric film reverses, the technique of using a ferroelectric for the dielectric film of the capacitor for information storage of a memory cell, and realizing ferroelectric memory of a non-volatile is developed. As for the nonvolatile memory (henceforth FRAM (Ferroelectric Random Access Memory)) using the ferroelectricity of the ferroelectric film, the application to a non-contact card (RF-ID:Radio Frequency-Identification) besides the general-purpose nonvolatile memory of a low power etc. is expected. SRAM (Static RAM) of existing [this nonvolatile memory], a flash memory, and DRAM (Dynamic RAM) etc. -- if it places and replaces, a large thing has that meaning.
[0003] It sets on the ferroelectric film of these and is PZT (SrBi2 Ta2 09 (Y1) of the stratified compound containing the ferroelectric containing Pb(s), such as Pb (Zr and Ti03), PLZT (Pb, La) (03) (Zr, Ti), and PLT (Pb, La) (Ti03), or Bi are known.) as a ferroelectric. Current [FRAM] uses many methods (henceforth 2T / 2C cel) which used two transistors and two capacitance as one cel. Of course, FRAM of 1T / 1C cel is also furthering research and development towards high integration. This 2T / 2C cel give an electrical potential difference to two capacitors in the combination of height, and performs writing and read-out by taking out the signal level corresponding to the electrical potential difference of the height on a capacitor to the data twisted pair line. Since it is full actuation actuation, it is stable. About a ferroelectric film ingredient, there are stabilization of the membraneous quality on production and a problem which should solve many in an imprint phenomenon, a fatigue property, etc. as a material property.
[0004] Drawing 12 is the sectional view of FRAM possessing the capacitor which has the ferroelectric film with the conventional ferroelectric property. the semi-conductor substrate 1 which consists of a p-type silicon semi-conductor etc. -- LOCOS (Local Oxidization of Silicon) -- SiO2 by law from -- the constituted component isolation region 2 is formed. n mold impurity diffusion field 3 used as the source / a drain field is formed in surface ****** going of the semi-conductor substrate 1. On between the source / drain field, the gate electrode 5 is formed through gate oxide (SiO2) 4. The gate electrode 5 consists of tungsten silicide film on for example, the polish recon film and the polish recon film, and the top face is protected by the silicon nitride. The semi-conductor substrate 1 is covered with the 1st insulator layer 6 which consists of BPSG (Born Phospharus Silicate Glass) film used as a middle insulator layer formed by the reduced pressure CVD method so that the gate electrode 5 might be

covered. The 1st insulator layer 6 is CMP (ChemicalMechanical Polishing). Flattening is ground and carried out. The 1st contact hole 61 and 61' are formed in the 1st insulator layer 6. Since the 1st insulator layer 6 by which flattening was carried out is about 790-890nm of thickness, the height of a contact hole is the same as this. The base is arranged for any contact hole to the impurity diffusion field 3 of the semi-conductor substrate 1. The connection wiring 71 and 71' are embedded at this contact hole 61 and 61'.

[0005] wiring -- 71 -- 71 -- ' -- the -- one -- contact -- a hole -- 61 -- 61 -- ' -- a side attachment wall -- forming -- having had -- Ti -- the film -- and -- the -- a top -- TiN -- the film -- from -- becoming -- the barrier -- metal -- a layer -- TiN -- the film -- a top -- a tungsten -- (-- W --) -- the film -- from -- constituting -- having -- **** . The source / drain field 3, gate oxide, and a gate electrode constitute Transistor Q. In order to control oxidation of the 1st contact hole 61 and the tungsten film embedded at 61', the middle insulator layer 7 is formed as a protective coat on the 1st insulator layer 6. The middle insulator layer 7 consists of silicon nitrides (although Si3 N4 and a chemical formula are this passage, since an atomic ratio changes somewhat in practice, it is written as SiN) formed by the reduced pressure CVD method of about 150nm of thickness. CVD (Chemical Vapour Deposition) -- law is the approach of forming a thin film on a semi-conductor substrate using heat energy, plasma discharge, etc. A reduced pressure CVD method is a means to change the inside of a reaction chamber into a reduced pressure condition, and to form membranes, and is performed on the conditions whose membrane formation temperature is 700-780 degrees C and whose membrane formation rates are a part for 0.8-1.5nm/. A plasma-CVD method is a means to make generate the plasma of low voltage reactant gas in a reaction chamber, and to form a thin film on a wafer by plasma decomposition. A reaction is performed at about 200-300 degrees C.

[0006] The ferroelectric capacitor C is formed on the middle insulator layer 7. Capacitor C contacts the middle insulator layer 7, and consists of layered products by which the sequential deposition of the dielectric film 92 and the up electrode 93 which consist of a lower electrode 91 plate line (PL) Connected and a ferroelectric which has a ferroelectric property was carried out. The lower electrode consists of Pt film formed on Ti film in contact with the middle insulator layer 7, and Ti film. The ferroelectric film 92 consists of for example, PZT film. The up electrode 93 consists of Pt film. The 2nd insulator layer 8 is formed on the middle insulator layer 7 so that Capacitor C may be covered. The 2nd insulator layer 8 consists of TEOS film (SiO2 which pyrolyzed organic oxy-silane Si(OC two H5) 4 called an abbreviated name TEOS, and was formed the film is said), and thickness is about 950nm. The 2nd insulator layer 8 is ground by CMP etc. and flattening is carried out. This the 2nd insulator layer 8 and middle insulator layer 7 are etched, and the 2nd contact hole 62 and 62' are formed of this etching. Since the 2nd insulator layer 8 by which flattening was carried out is 950nm of thickness, the 2nd contact hole 62 and the height of 62' are the same as this. The contact hole 62 of these 2nd and 62' are connected with the 1st contact hole 61 and 61', respectively, and wiring 72 and 72' which are embedded are also connected to wiring 71 and 71'. Wiring 72 and 72' consist of a barrier metal layer which consists of Ti film formed in the 2nd contact hole 62 and the side attachment wall of 62', and TiN film on it, and tungsten film on it.

[0007] Wiring 10 and 10' are formed on the 2nd insulator layer 8. Wiring 10 and 10' which the 2nd insulator layer 8 was made to carry out the sequential deposition of Ti film, the TiN film, aluminum film, and the TiN film, carried out patterning of this, and consisted of a lower layer barrier metal layer (Ti film / TiN film) / aluminum film / an upper barrier metal layer (TiN film) are formed. This wiring 10 and 10' are the 1st-layer aluminum wiring on the semi-conductor substrate 1. The 3rd insulator layer 9 is formed on the 2nd insulator layer 8 so that wiring 10 and 10' may be covered. The 3rd insulator layer 9 consists of TEOS film, and thickness is about 1240nm. The 3rd insulator layer 9 is ground by CMP etc. and flattening is carried out. This 3rd insulator layer 9 is etched and the 3rd contact hole 11 from that front face to [with this etching process] the top face of wiring 10 and 10' and 11' are formed. Since the thickness of the 3rd insulator layer 9 by which flattening was carried out is 1240nm and the thickness of wiring 10 and 10' is about 520nm, the 3rd contact hole 11 and the height of 11' are about 720nm. The 3rd contact hole 11, the wiring 12 currently embedded at 11', and 12' are connected to the connection

wiring 72 and 72', respectively. The connection wiring 12 and 12' consist of the 3rd contact hole 11 and tungsten film embedded at 11'.

[0008] Wiring 13 and 13' are formed on the 3rd insulator layer 9. Wiring 13 and 13' which the 3rd insulator layer 9 was made to carry out the sequential deposition of Ti film, the TiN film, aluminum film, and the TiN film, carried out patterning of this, and consisted of a lower layer barrier metal layer (Ti film / TiN film) / aluminum film / an upper barrier metal layer (TiN film) are formed. This wiring 13 and 13' are the 2nd-layer aluminum wiring on the semi-conductor substrate 1. It is covered with the protection insulator layers 14, such as a silicon nitride formed by the plasma-CVD method on the front face of the 3rd insulator layer 9 so that wiring 13 and 13' might be covered. Wiring 13 is connected to the up electrode 93 of Capacitor C, and wiring 13' is connected to the bit line (BT). Drawing 4 is a FRAM cel circuit diagram on the conventional semi-conductor substrate.

[0009]

[Problem(s) to be Solved by the Invention] As mentioned above, in order to control scaling of the tungsten usually embedded at the 1st contact hole, the silicon nitride (SiN) which is precise on the front face and has oxidation resistance in it is made to deposit, and the TEOS film is made to deposit as an interlayer insulation film on it. When forming the 2nd contact hole on this 1st contact hole, it is reactive ion etching about the TEOS film. (RIE:Reactive Ion Etching) It etches perpendicularly. It is made for the conditions at that time to have the 10 more than selection ratio of the TEOS film and a silicon nitride. And the terminal point of the RIE is carried out in the interface of the TEOS film and a silicon nitride, or a silicon nitride. Next, the silicon nitride on the tungsten film in a contact hole is etched by RIE, the terminal point of the etching is carried out by the tungsten film interface, and the 2nd contact hole is formed.

[0010] if the silicon nitride (SiN) deposited with the reduced pressure CVD method is used for the mask of etching in the case of forming the 2nd contact hole here -- an elevated temperature (700 degrees C or more) -- and it is spread to the impurity diffusion field which the tungsten ran through the barrier metal layer (Ti film / TiN film) for the reasons nil why an etch rate is slow etc. at the bottom corner of the 1st contact hole, and was formed in the semi-conductor substrate, and has a bad influence on the electrical characteristics of a transistor. Moreover, if RIE is carried out after the doubling gap of a reticle has arisen in PEP of the 2nd contact hole, the problem that the 2nd contact hole runs [etching] even to a semi-conductor substrate will arise. This invention is made according to such a situation, offers the manufacture approach of a semiconductor memory of providing the 1st and 2nd contact holes with which the phenomenon which the connection wiring material in the 1st contact hole runs through a barrier metal layer, and diffuses inside an impurity-diffusion field was controlled, and offers the semiconductor memory with which the capacitor formed between the insulator layers in which the 1st and 2nd contact holes were formed is arranged between insulator layers at stability.

[0011]

[Means for Solving the Problem] This invention is inserted between the insulator layers in which the 1st and 2nd contact holes were formed, and is characterized by using the insulator layer which consisted of a silicon nitride formed by the reduced pressure CVD method as a middle insulator layer used for the mask at the time of etching the 2nd contact hole, and a silicon nitride formed by the plasma-CVD method. Moreover, when the lower electrode of said capacitor formed on a middle insulator layer consists of titanium (Ti) film and platinum (Pt) film formed on this, it is characterized by arranging the TEOS film formed by the reduced pressure CVD method between the titanium film and a middle insulator layer. Since a plasma-CVD method is processed at low temperature (about 200-300 degrees C), it becomes, without destroying the barrier metal layer formed in the 1st contact hole, and does not activate diffusion of connection wiring of a tungsten etc. Moreover, since the TEOS film by the reduced pressure CVD method has good concordance with the titanium film or the platinum film, if such TEOS film is made to deposit on a middle insulator layer, the capacitor by which the electrical property was stabilized will be formed, without stabilizing a capacitor and spoiling the electrical characteristics.

[0012] Namely, the transistor for a switch by which the semiconductor memory of this invention was formed in the semi-conductor substrate and said semi-conductor substrate, and a drain or the source was

connected to the bit line, The 1st insulator layer formed on said semi-conductor substrate so that said transistor for a switch might be covered, The 1st electrode which was formed on the middle insulator layer formed on said 1st insulator layer, and said middle insulator layer, and was connected to the source or the drain of said transistor for a switch, So that the capacitor for charge storages equipped with the 2nd electrode and dielectric film which contacted said middle insulator layer and were connected to the plate line, and said capacitor for charge storages may be covered Wiring which connects electrically said drain or source, and said 1st electrode through the 2nd contact hole formed in the 2nd insulator layer formed on said middle insulator layer, and the 1st contact hole and said 2nd insulator layer formed in said 1st insulator layer is provided. Said middle insulator layer It is characterized by consisting of a silicon nitride formed by the reduced pressure CVD method, and a silicon nitride formed by the plasma-CVD method.

[0013] The dielectric film which consists of a ferroelectric which has a ferroelectric property may be used for said capacitor. Said middle insulator layer is sandwiched by the 1st [which was formed by the reduced pressure CVD method], 2nd silicon nitride and said 1st [the], and 2nd silicon nitrides, and may be made to consist of the 3rd silicon nitride formed by the plasma-CVD method. The laminating of two or more silicon nitrides from which a class differs continuously easily only by changing conditions suitably in a CVD reaction chamber is carried out. Said middle insulator layer may be thickness (135nm thru/or 165nm), and you may make it the total thickness of the 1st and 2nd silicon nitrides be 10nm thru/or 20nm. Said 1st contact hole side attachment wall is perpendicularly formed to said 1st insulator layer, and the side attachment wall is formed in the shape of a taper to said 2nd insulator layer, and you may make it said 2nd contact hole have area with opening larger than a base. When forming the 2nd contact hole, a contact hole which breaks through the 2nd insulator layer by etching and reaches a semi-conductor substrate is not formed.

[0014] Said 1st insulator layer of the part which touches the inferior surface of tongue of said middle insulator layer consists of TEOS film formed by the plasma-CVD method, and other parts may be made to consist of BPSG film. When embedding connection wiring in the 1st contact hole and using CMP, the gate electrode which grinds the BPSG film with a quick polish rate too much, and is embedded at the 1st insulator layer is not damaged. You may make it the TEOS film formed by the reduced pressure CVD method intervene between said capacitors and said middle insulator layers. Since this TEOS film can make the lower electrode of the capacitor which uses the ferroelectric film deposit with a sufficient stacking tendency, it can grow up the ferroelectric film with a sufficient stacking tendency on this lower electrode. Said 2nd electrode of said capacitor consists of titanium film and platinum film formed on this, and this titanium film may be made to be formed in contact with the TEOS film formed by said reduced pressure CVD method. You may make it the TEOS film which said middle insulator layer is thickness (135nm thru/or 165nm), and was formed by said reduced pressure CVD method have 200nm thickness. On said ferroelectric film with which said 1st electrode of said capacitor is formed on said ferroelectric film, and said 1st electrode top and said 1st electrode are not formed, the protective coat which consists of the same ingredient as said ferroelectric film may be made to be formed. Since the ferroelectric film is used as a protective coat which covers an up electrode, the ferroelectric film is formed with a sufficient stacking tendency.

[0015] Moreover, the process at which the manufacture approach of the semiconductor memory of this invention forms in a semi-conductor substrate the transistor for a switch by which a drain or the source was connected to the bit line, The process which forms the 1st insulator layer on said semi-conductor substrate so that said transistor for a switch may be covered, The process which forms the 1st contact hole which etches said 1st insulator layer and results in the drain or the source of said semi-conductor substrate, The process which embeds connection wiring in said 1st contact hole, and the process which forms a middle insulator layer on said 1st insulator layer so that connection wiring in said 1st contact hole may be covered, So that the process which forms the capacitor for charge storages equipped with the dielectric film inserted into the 1st electrode, 2nd electrode, and these electrodes on said middle insulator layer, and said capacitor for charge storages may be covered The process which forms the 2nd insulator layer on said middle insulator layer, and the process which forms the 2nd contact hole which

etches said the 2nd insulator layer and said middle insulator layer, and results in connection wiring in said 1st contact hole, Connection wiring in the process which embeds connection wiring in said 2nd contact hole, and said 1st and 2nd contact holes is included. The process which forms wiring which connects electrically said drain or source, and said 1st electrode through said 1st contact hole and said 2nd contact hole is provided. Said middle insulator layer is characterized by consisting of a silicon nitride formed by the reduced pressure CVD method, and a silicon nitride formed by the plasma-CVD method.

[0016]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of invention is explained with reference to a drawing. First, the 1st example is explained with reference to drawing 1 , drawing 6 , or drawing 10 . The sectional view of a ferroelectric RAM (FRAM) is shown in drawing 1 . MOS transistor Q is formed in the p-type silicon semi-conductor substrate 100. MOS transistor Q consists of the source / a drain field 103 which consists of an n mold impurity diffusion field, gate oxide 104, and gate electrode 105 grade. The gate electrode 105 is connected to a word line (WL). On this MOS transistor Q, the interlayer insulation film (the 1st insulator layer) 106 is formed. The 1st insulator layer 106 consists of BPSG film formed by the reduced pressure CVD method. SiO2 according to LOCOS in the semi-conductor substrate 100 which consists of a p-type silicon semi-conductor etc. from -- the constituted component isolation region 102 is formed. n mold impurity diffusion field 103 used as the source / a drain field is formed in the surface field of the semi-conductor substrate 100. On between the source / drain field, the gate electrode 105 is formed through gate oxide (SiO2) 104. The gate electrode 105 consists of tungsten silicide film on for example, the polish recon film and the polish recon film, and this silicide film top face is protected by the silicon nitride.

[0017] The semi-conductor substrate 100 is covered with the 1st insulator layer (interlayer insulation film) 106 which consists of BPSG film formed by the reduced pressure CVD method so that the gate electrode 105 may be covered. The 1st insulator layer 106 is ground by CMP and flattening is carried out. The 1st contact hole 161 and 161' are formed in this 1st insulator layer 106. First, RIE etching of the BPSG film front face is carried out using the mixed gas which consists of CHF3+O2+CO, and, subsequently it is O2. CF4 The 1st contact hole 161 and 161' which perform trench etching to the part which carried out opening by RIE etching by mixed gas (one or more flow rate) further, and have a perpendicular side attachment wall are formed. Since the 1st insulator layer 106 by which flattening was carried out is about 790-890nm of thickness, it is the same as this. [of the 1st contact hole 161 and the height of 161'] The base is arranged for any contact hole to the impurity diffusion field 103 of the semi-conductor substrate 100. The connection wiring 171 and 171' are embedded at this 1st contact hole 161 and 161'. connection -- wiring -- 171 -- 171 -- ' -- the -- one -- contact -- a hole -- 161 -- 161 -- ' -- a side attachment wall -- forming -- having had -- Ti -- the film -- and -- the -- a top -- TiN -- the film -- from -- becoming -- the barrier -- metal -- a layer -- TiN -- the film -- a top -- a tungsten -- (-- W --) -- the film -- from -- constituting -- having -- **** . The source / drain field 103, gate oxide 104, and the gate electrode 105 constitute Transistor C.

[0018] Connection wiring makes Ti film of about 40nm of thickness, and the TiN film of about 60nm of thickness deposit with the usual deposition techniques, such as high-melting long sputtering, one by one on the 1st insulator layer 106 also including the inside of the 1st contact hole, and makes about 620nm of tungstens deposit in the shape of a blanket on it. And 300 more degree-Cx 60 minutes, and N2 Crystallization processing is performed in an ambient atmosphere. While removing the layered product on the 1st insulator layer 106 other than the ingredient which deposited these layered products in the 1st contact hole 161 and 161' after that by the approach including the CMP method, or CDE (Chemical Dry Etching) and a micro Usher process etc., flattening of the front face of the 1st insulator layer 106 is carried out. In order to control oxidation of the 1st contact hole 161 and the tungsten embedded at 161', thickness forms the middle insulator layer 107 which is 135-165nm as a protective coat on the 1st insulator layer 106. The middle insulator layer 107 consists of a silicon nitride (PCVDSiN) formed by the plasma-CVD method, and a silicon nitride (LPCVDSiN) formed by the reduced pressure CVD method.

[0019] The silicon nitride formed by the reduced pressure CVD method makes dichlorosilane and ammonia react on the temperature of 700-780 degrees C, and conditions with a pressure of 20-100Pa, and is made to deposit on the 1st insulator layer. The silicon nitride formed by the plasma-CVD method is SiH4-NH3 as reactant gas. It uses, and substrate temperature is made to react on the conditions which call 0.2Torr(s) about 200-300 degrees C and a pressure, and call a growth rate 30 nm/min, and is deposited on an insulator layer.
[0020] Here, the detail of a middle insulator layer is explained, referring to drawing 6 and drawing 7 . The sectional view of the semi-conductor substrate which has the middle insulator layer by which drawing 6 was formed on the contact hole, and drawing 7 are the sectional views of the semi-conductor substrate which has the middle insulator layer formed on the conventional contact hole. The 1st contact hole 161 was formed by RIE etching and trench etching as mentioned above, and the pars basilaris ossis occipitalis has entered into the impurity diffusion field 103 formed in the semi-conductor substrate 100. The part to which the 1st insulator layer 106 is in contact with the semi-conductor substrate 100 although most consists of BPSG film 106A consists of same oxide-film 106B as gate oxide. Therefore, since the etching rates of BPSG film 106A, oxide film 106B, and the impurity diffusion field 103 differ, the path of a contact hole changes with depth. In the conventional etching approach, as a contact hole cross section is shown in drawing 7 , it is larger than the part of oxide-film 6B, a part, i.e., near a pars basilaris ossis occipitalis, the impurity diffusion field 3. In such the condition, barrier metal layer 71B to which a side attachment wall and a pars basilaris ossis occipitalis adhere in sputtering is not formed near the corner of a pars basilaris ossis occipitalis, but the tungsten film 71A part of the connection wiring 71 touches the direct semi-conductor substrate 1. Therefore, the diffusion to the semi-conductor substrate 1 of a tungsten was remarkable.
[0021] however -- this example -- above -- O2 CF4 Since it is alike by performing trench etching using mixed gas (more than flow rate 1 (O2 >CF4)) and over etching of the silicon is not carried out, an almost perpendicular side attachment wall is formed [near the pars basilaris ossis occipitalis of a semi-conductor substrate part]. Therefore, the parts of BPSG film 106A and the impurity diffusion field 103 are substantially perpendicular, the part between both in whom oxide-film 106B exists inclines, and the side attachment wall of the 1st insulator layer 106 becomes the configuration which moreover wears a base corner section radius of circle, and has predetermined R. If the internal configuration of a contact hole is such, it will be lost that the barrier metal ingredient performed by sputtering accumulates on the whole side attachment wall at homogeneity, barrier metal layer 171B, as a result, interrupts tungsten film 171A and the impurity diffusion field 103 of the semi-conductor substrate 100, and both touch directly. A reduced-pressure CVD method is a means changes the inside of a reaction chamber into a reduced-pressure condition, and form membranes, it carries out on the conditions whose membrane-formation temperature is 700-780 degrees C and whose membrane-formation rates are a part for 0.8-1.5nm/, and a plasma-CVD method generates the plasma of low-voltage reactant gas in a reaction chamber, and a reaction is performed at about 200-300 degrees C in the CVD method which forms a thin film on a semi-conductor substrate by means form a thin film on a wafer by plasma decomposition.
[0022] After embedding the connection wiring 171 at this 1st contact hole 161, the middle insulator layer 107 is formed in the 1st insulator layer 106. The middle insulator layer 107 consists of CVD film of three layers. The 1st layer Silicon nitride (LPCVDSiN) 107A formed by the reduced pressure CVD method whose thickness is about 10-20nm, and the 2nd layer Silicon nitride (PCVDSiN) 107B formed by the plasma-CVD method thickness is about 110-130nm, and the 3rd layer consist of silicon nitride (LPCVDSiN) 107C formed by the reduced pressure CVD method whose thickness is about 10-20nm.
[0023] Furthermore drawing 8 and drawing 9 are added, and explanation of drawing 1 is continued. The sectional view of the semi-conductor substrate which has a capacitor on the middle insulator layer by which drawing 8 was formed on the contact hole, and drawing 9 are the top views showing the capacitor on a middle insulator layer. The ferroelectric capacitor C is formed on the middle insulator layer. In this example, TEOS film 107D by the reduced pressure CVD method is further formed as a middle insulator layer on the middle insulator layer 107. Of course, existence of such middle insulator layer 107D may not have this at this invention rather than may be indispensable. Middle insulator layer 107D consists of

TEOS film formed by the reduced pressure CVD method, and thickness is about 200nm. In this example, the direct capacitor is carried on this TEOS film 107D. Capacitor C consists of layered products by which the sequential deposition of the dielectric film 192 and the up electrode 193 which consist of a lower electrode 191 connected with PL which touches TEOS film 107D directly, and a ferroelectric which has a ferroelectric property was carried out.

[0024] The lower electrode 191 consists of Pt film 191A whose thickness which was formed by sputtering etc. and formed on Ti film 191B whose thickness in contact with middle insulator layer 107D is about 20nm, and Ti film 191B is about 175nm. the ferroelectric film 192 -- from for example, the PZT film or the tantalic acid niobic acid strontium bismuth (SBT:SrBi2 2 (Nb, Ta) O9) film -- becoming -- a sol-gel method, the sputtering method, and MOCVD -- it is formed using law etc. The thickness of the ferroelectric film 192 is about 240nm. The up electrode 193 consists of Pt film of about 175nm of thickness, and is formed by the sputtering method. Patterning of the layered product which constitutes these capacitors is carried out one by one, and it is orthopedically operated by capacitor structure. The up electrode 193 has an area smaller than the ferroelectric film 192, and the protective coat 194 which consists of the same ingredient as the ferroelectric film is formed on the ferroelectric film 192 so that this up electrode 193 may be covered. Even if the ferroelectric film 192 is manufacturing by this protective coat 194 and it is after manufacture, it exists, where a ferroelectric property is stabilized. The 2nd insulator layer 108 is formed on the middle insulator layers 107 and 107D so that Capacitor C may be covered. The 2nd insulator layer 108 consists of TEOS film formed by the plasma-CVD method, and thickness is about 1200nm.

[0025] The 2nd insulator layer 8 is ground by CMP etc. and flattening is carried out. First, these the 2nd insulator layer 108 and middle insulator layers 107 and 107D perform trench etching for the 2nd insulator layer 108 using the mixed gas of C4 F8+CO+Ar, form opening, subsequently perform RIE etching continuously, and form the 2nd contact hole 162 and 162'. After that, in the 2nd contact hole 162 and 162', Ti film of 40nm of thickness and the TiN film of 60nm of thickness are covered with high-melting sputtering, further, the tungsten film is made to deposit on the TiN film, and the connection wiring 172 and 172' are formed. Flattening of the 2nd insulator layer 108 is carried out, and since the thickness is about 1200nm, the 2nd contact hole 162 and the height of 162' of it are the same as this. The contact hole 162 of these 2nd and 162' are connected with the 1st contact hole 161 and 161', respectively, and wiring 172 and 172' which were embedded are also connected to wiring 171 and 171'. Wiring 110 and 110' are formed on the 2nd insulator layer 108. Wiring 110 and 110' which the 2nd insulator layer 108 was made to carry out the sequential deposition of Ti film, the TiN film, aluminum film, and the TiN film, carried out patterning of this, and consisted of a lower layer barrier metal layer (Ti film / TiN film) / aluminum film / an upper barrier metal layer (TiN film) are formed. This wiring 110 and 110' are the 1st-layer aluminum wiring on the semi-conductor substrate 1 (1aluminum). The 3rd insulator layer 109 is formed on the 2nd insulator layer 108 so that wiring 110 and 110' may be covered. The 3rd insulator layer 109 consists of TEOS film formed by the plasma-CVD method, and the thickness is about 1240nm.

[0026] The 3rd insulator layer 109 is ground by CMP etc. and flattening is carried out. The 3rd insulator layer 109 is etched and wiring 110, the 3rd contact hole 111 which reaches the top face of 110', and 111' are formed from the front face. Since the thickness of the 3rd insulator layer 9 by which flattening was carried out is 1240nm and the thickness of wiring 110 and 110' is about 520nm, the 3rd contact hole 111 and the height of 111' are about 720nm. The 3rd contact hole 111, the wiring 112 currently embedded at 111', and 112' are connected to the connection wiring 172 and 172' through wiring 110 and 110', respectively. The connection wiring 112 and 112' consist of the 3rd contact hole 111 and tungsten film formed in 111'. Moreover, wiring 113 and 113' are formed on the 3rd insulator layer 109. Wiring 113 and 113' which the 3rd insulator layer 109 was made to carry out the sequential deposition of Ti film, the TiN film, aluminum film, and the TiN film, carried out patterning of this, and consisted of a lower layer barrier metal layer (Ti film / TiN film) / aluminum film / an upper barrier metal layer (TiN film) are formed. This wiring 113 and 113' are the 2nd-layer aluminum wiring on the semi-conductor substrate 1 (2aluminum). It is covered with the protection insulator layers 114, such as a silicon nitride

formed by the plasma-CVD method on the 3rd insulator layer 109 so that wiring 113 and 113' might be covered. Wiring 113 is connected to the up electrode 93 of Capacitor C, and wiring 113' is connected to the bit line (BL).
[0027] If said etching gas for forming the 1st contact hole is used, the configuration where the base corner edge part of a contact hole was square will turn into a configuration which is roundish and has an R (R), and the coverage of a barrier metal layer will improve. Moreover, the thrust omission of the barrier metal layer of the tungsten in the base corner edge part of the 1st contact hole can be controlled under the effect of thermal stress by making it a three-tiered structure using the silicon nitride which was formed by the plasma-CVD method in addition to the silicon nitride conventionally formed with the reduced pressure CVD method.
[0028] Here, the process which forms the 2nd contact hole with reference to drawing 10 is explained. In the process which etches the 2nd contact hole 162 by RIE, since there is 10 more than etch selectivity of the 2nd insulator layer (TEOS film) 108 and the middle insulator layer (silicon nitride) 107, by the first trench etching, etching progresses forming a back taper and etching carries out a terminal point middle insulator layer 107 front face or in it. Next, if RIE etching is performed, etching will carry out the terminal point of this middle insulator layer by the tungsten interface of the 1st contact hole front face. Since the tip of the 2nd contact hole 162 etched even if it doubles with the 1st contact hole and a gap arises since it is etched in the shape of a back taper runs against the side attachment wall of the 1st contact hole 161 at one of parts, the 2nd contact hole 162 is not dug even in the semi-conductor substrate 100. Therefore, if thickness management of the 2nd insulator layer 108 and the middle insulator layer 107 is performed enough, successive reaction nature etching will be attained easily. Moreover, also after the reticle doubling gap with the 1st contact hole 161 and the 2nd contact hole 162 has occurred, it also becomes possible to control etching time to carry out the terminal point of the successive reaction nature ion etching into the BPSG film of the 1st insulator layer 106.
[0029] The case where deposited and processed the ferroelectric film of a FRAM capacitor into what deposited the TEOS film (henceforth the PTEOS film) and lower electrode by the plasma-CVD method on the silicon nitride formed with the reduced pressure CVD method, and a capacitor is formed is assumed. After this, the ferroelectric film adds heat treatment in order to usually stabilize the crystal structure. Heat treatment is 650 degree-Cx 60 minutes, and O2. Like the heat process performed in an ambient atmosphere, it is 650 degree-Cx5 seconds -> 850-degree-Cx 5 seconds, and O2. The process in an ambient atmosphere is performed. However, since the difference of thermal expansion is large, film peeling, nebula, etc. generate the PTEOS film and Ti film in the interface of the PTEOS film and Ti film. Moreover, if heat treatment among said oxygen ambient atmosphere after forming the lower electrode which consists of Ti film and Pt film on it and depositing and processing the ferroelectric film of a FRAM capacitor on a silicon nitride is added, a thermal stress rearrangement will occur from the difference in the temperature distribution in a wafer. In this example, when heat expansion makes the LPTEOS film near Ti film intervene between a lower electrode and a middle insulator layer, it is rare for that film peeling and nebula to arise, and is making.
[0030] Furthermore, in heat treatment performed immediately after, for example, depositing and processing the ferroelectric film which consists of PZT, the lead contained in the ferroelectric film may invade into the interface of a lower electrode and the LPTEOS film, may react with oxygen, lead glass (PbO-SiO2) may be generated, and this lead glass may cause membraneous degradation of film peeling etc. For this reason, in this example, after membrane formation of the LPTEOS film, the thermal oxidation process of about [700 degree-Cx30 minute] hydrogen burning can be added, the membraneous quality of the LPTEOS film can be raised, and the stacking tendency of a lower electrode can be improved. This is for the titanium silicide film which does so the operation which prevents that lead glass invades into the film down of a lower electrode to generate to the interface of the LPTEOS film and Ti film. Since a plasma-CVD method is processed at low temperature, it becomes, without destroying the barrier metal layer formed in the 1st contact hole, and does not activate diffusion of connection wiring of a tungsten etc. Moreover, it leads to the improvement in membraneous which deposits Ti film on the TEOS film by the reduced pressure CVD method, a capacitor is stabilized, and

the electrical characteristics are not spoiled. Furthermore, since the TEOS film by the reduced pressure CVD method can be formed with a sufficient stacking tendency and can improve the stacking tendency of Ti film on it, it can improve the stacking tendency of the ferroelectric film on a lower electrode.
[0031] Next, the 2nd example is explained with reference to drawing 11 . The description is in the approach of forming connection wiring embedded the 1st contact hole of a semiconductor memory, and into it in this example, and drawing 11 is the sectional view of a production process showing the semi-conductor substrate in which the 1st contact hole was shown. Since the structure of the middle insulator layer formed on the 1st contact hole, the 2nd insulator layer, the 2nd contact hole, etc. is the same as the 1st example, explanation is omitted. for example, SiO2 according to LOCOS in the semi-conductor substrate 200 which consists of a p-type silicon semi-conductor etc. from -- the constituted component isolation region is formed. n mold impurity diffusion field 203 used as the source / a drain field is formed in the surface field of the semi-conductor substrate 200. On between the source / drain field, the gate electrode is formed through gate oxide (SiO2). A gate electrode consists of tungsten silicide film on for example, the polish recon film and the polish recon film, and this silicide film top face is protected by the silicon nitride. The semi-conductor substrate 200 is covered with the 1st insulator layer (interlayer insulation film) 206 which has the BPSG film by the reduced pressure CVD method so that a gate electrode may be covered. The 1st insulator layer 206 is ground by CMP and flattening is carried out. Next, the TEOS film 207 by the thin plasma-CVD method of about 100nm of thickness is formed on this 1st insulator layer 206.
[0032] The 1st contact hole 261 is formed in the TEOS film 207 and the 1st insulator layer 206 by this plasma-CVD method. First, RIE etching of the TEOS film by the plasma-CVD method and the BPSG film front face by the reduced pressure CVD method is carried out using the mixed gas which consists of CHF3+O2+CO, and, subsequently it is O2. CF4 The 1st contact hole 261 which performs trench etching to the part which carried out opening by RIE etching by mixed gas (one or more flow rate) further, and has a perpendicular side attachment wall is formed. As for the 1st contact hole 261, the base is arranged to the impurity diffusion field 203 of the semi-conductor substrate 100. Next, barrier metal layer 271B which consists of Ti film of about 40nm of thickness and TiN film of about 60nm of thickness is deposited in high-melting long sputtering etc. one by one, and tungsten film 271A of about 620nm of thickness is made to deposit on it also including the inside of the 1st contact hole 261 on the 1st insulator layer 206 and the TEOS film 207 by the plasma-CVD method. Then, these layered products are ground by the CMP method etc., and the unnecessary layered product ingredient is removed. And it leaves the ingredient deposited in the 1st contact hole 261, and the layered product ingredient on the TEOS film 207 by the other plasma-CVD method is removed.
[0033] Since the polish rate is smaller than the BPSG film by the reduced pressure CVD method enough, the TEOS film by the plasma-CVD method can control a phenomenon which damages the gate electrode which ground the BPSG film by the reduced pressure CVD method by exaggerated polishing, for example, was formed on the semiconductor device isolation region and which was generated well conventionally. Thus, the connection wiring 271 which consisted of 271B and tungsten film 271A which consist of Ti film and TiN film is embedded at the 1st contact hole 261. Since formation of the process after this, the middle insulator layer formed on the 1st contact hole, the 2nd insulator layer, the 2nd contact hole, etc. is the same as the 1st example, explanation is omitted. ** characterized by using the insulator layer which consisted of a silicon nitride formed by the reduced pressure CVD method as a middle insulator layer used for the mask at the time of being inserted also in this example between the insulator layers in which the 1st and 2nd contact holes were formed, and etching a contact hole, and a silicon nitride formed by the plasma-CVD method. Since a plasma-CVD method is processed at low temperature, destroying the barrier metal layer formed in the 1st contact hole of it is lost, and it does not activate diffusion of connection wiring of a tungsten etc.
[0034] As mentioned above, since this invention relates to the structure of the middle insulator layer inserted in the middle of the contact hole of two-step structure in order to control scaling, it is applicable to any semiconductor devices, such as memory and logic. It is optimal to apply to the semiconductor device equipped with the ferroelectric film which has ferroelectric properties, such as a ferroelectric

RAM (FRAM), especially. Hereafter, the actuation is explained about the semiconductor memory explained in the 1st and 2nd examples with reference to drawing 2 thru/or drawing 5 , i.e., FRAM. The circuit diagram of a FRAM cel where the hysteresis characteristic Fig. of a condition which is not desirable as a FRAM cel as for the hysteresis characteristic Fig. in which drawing 2 shows the applied voltage / polarization property of the ferroelectric film, and drawing 3 , and drawing 4 explain write-in actuation of FRAM, and drawing 5 are the potential variation diagrams of the plate electrode PL at the time of the writing of a FRAM cel. The applied voltage / polarization property of ferroelectric thin films, such as PZT film, are shown in drawing 2 . A ferroelectric thin film has a hysteresis characteristic, as shown in drawing 2 . And data are memorizable whether the remanence Pr in the condition, i.e., the condition of V= 0 (V), of not impressing an electrical potential difference is "forward", or it is "negative."

[0035] Drawing 3 is a hysteresis characteristic which is not desirable as a ferroelectric memory cell of FRAM. That is, Remanence Pr is very small, consequently the problem of data disappearing easily by the disturbance from the outside to which the read-out margin by the sense amplifier falls exists. The property shown in drawing 3 is a hysteresis characteristic in a 80-degree C elevated-temperature condition. Then, write-in actuation of the memory cell using a ferroelectric thin film is explained using drawing 4 and drawing 5 . The ferroelectric RAM using a FRAM cel constitutes one memory cell with two MOS transistors Q1 and Q2 and ferroelectric capacitors C1 and C2. As shown in the condition C1 of drawing 4 (a), i.e., a capacitor, at the arrow head of the drawing Nakagami sense, and above polarization As (forward polarization is called hereafter) shows a capacitor C2 at the arrow head of the drawing Nakashita sense, down polarization The condition that (negative polarization is called hereafter) has appeared is defined as "1", and the condition that negative polarization appears in the condition C1 of drawing 4 (b), i.e., a capacitor, and forward polarization has appeared in the capacitor C2 is defined as "0."

[0036] ("1" write-in actuation) The step in the case of writing "1" in a memory cell is shown hereafter. First, 5V are impressed to a bit line BL, and it is a bit line. 0V are impressed to /BL ("/" is the same the following showing a reversal signal). And 7V are impressed to a word line WL, and 0V are impressed to the plate electrode PL. A capacitor C1 is in the condition of a of drawing 2 , and this condition has a capacitor C2 in the condition of b of drawing 2 . Then, PL is set to 5V. Consequently, a capacitor C1 will be in the condition of b of drawing 2 , and a capacitor C2 will be in the condition of c of drawing 2 R> 2. Then, PL is set to 0V. Consequently, a capacitor C1 will be in the condition of a of drawing 2 , and a capacitor C2 will be in the condition of d of drawing 2 . It writes in drawing 5 and change of the potential (VPL) of the plate electrode PL at the time is shown. Forward polarization appears in the condition C1 of drawing 4 (a), i.e., a capacitor, as mentioned above, negative polarization appears in a capacitor C2, and "1" writing is realized.

[0037] ("0" write-in actuation) The step in the case of writing "0" in a memory cell is shown hereafter. First, 0V are impressed to a bit line BL, and it is a bit line. 5V are impressed to /BL. And 7V are impressed to a word line WL, and 0V are impressed to the plate electrode PL. In this condition, a capacitor C1 is in the condition of b of drawing 2 , and a capacitor C2 is in the condition of a of drawing 2 R>2 **. Then, PL is set to 5V. Consequently, a capacitor C1 will be in the condition of c of drawing 2 , and a capacitor C2 will be in the condition of b of drawing 2 . Then, PL is set to 0V. Consequently, a capacitor C1 will be in the condition of d of drawing 2 , and a capacitor C2 will be in the condition of a of drawing 2 . Negative polarization appears in the condition C1 of drawing 4 (b), i.e., a capacitor, as mentioned above, forward polarization appears in a capacitor C2, and "0" writing is realized. Since the above FRAMs have small power consumption, they are used for non-power-source ID equipments, such as RFID, etc.

[0038]

[Effect of the Invention] A plasma-CVD method becomes without destroying the barrier metal layer formed in the 1st contact hole, since it processes at low temperature, and does not activate diffusion of connection wiring of a tungsten etc. further. Moreover, since the TEOS film by the reduced pressure CVD method has good concordance with Ti film or Pt film, if such TEOS film is made to deposit on a

middle insulator layer, since a capacitor will be stabilized and the electrical characteristics will not be spoiled, the semiconductor memory by which electrical characteristics were stabilized, and its manufacture approach can be acquired.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] A semi-conductor substrate and the transistor for a switch by which it was formed in said semi-conductor substrate, and a drain or the source was connected to the bit line, The 1st insulator layer formed on said semi-conductor substrate so that said transistor for a switch might be covered, The 1st electrode which was formed on the middle insulator layer formed on said 1st insulator layer, and said middle insulator layer, and was connected to the source or the drain of said transistor for a switch, So that the capacitor for charge storages equipped with the 2nd electrode and dielectric film which contacted said middle insulator layer and were connected to the plate line, and said capacitor for charge storages may be covered Wiring which connects electrically said drain or source, and said 1st electrode through the 2nd contact hole formed in the 2nd insulator layer formed on said middle insulator layer, and the 1st contact hole and said 2nd insulator layer formed in said 1st insulator layer is provided. Said middle insulator layer The semiconductor memory characterized by consisting of a silicon nitride formed by the reduced pressure CVD method, and a silicon nitride formed by the plasma-CVD method.
[Claim 2] Said capacitor is a semiconductor memory according to claim 1 characterized by having the dielectric film which consists of a ferroelectric which has a ferroelectric property.
[Claim 3] Said middle insulator layer is a semiconductor memory according to claim 1 characterized by consisting of the 3rd silicon nitride which was sandwiched by the 1st [which was formed by the reduced pressure CVD method], 2nd silicon nitride and said 1st [the], and 2nd silicon nitrides, and was formed by the plasma-CVD method.
[Claim 4] Said 2nd contact hole is a semiconductor memory according to claim 1 to 3 with which it is characterized by forming perpendicularly said 1st contact hole side attachment wall to said 1st insulator layer, and forming the side attachment wall in the shape of a taper to said 2nd insulator layer, and opening having an area larger than a base.
[Claim 5] The semiconductor memory according to claim 2 characterized by the TEOS film formed by the reduced pressure CVD method intervening between said capacitors and said middle insulator layers.
[Claim 6] It is the semiconductor memory according to claim 5 which said 2nd electrode of said capacitor consists of titanium film and platinum film formed on this, and is characterized by forming this titanium film in contact with the TEOS film formed by said reduced pressure CVD method.
[Claim 7] Said 1st electrode of said capacitor is a semiconductor memory according to claim 5 or 6 characterized by forming the protective coat which consists of the same ingredient as said ferroelectric film on said ferroelectric film with which it is formed on said ferroelectric film, and said 1st electrode top and said 1st electrode are not formed.
[Claim 8] The process which forms in a semi-conductor substrate the transistor for a switch by which a drain or the source was connected to the bit line, The process which forms the 1st insulator layer on said semi-conductor substrate so that said transistor for a switch may be covered, The process which forms the 1st contact hole which etches said 1st insulator layer and results in the drain or the source of said semi-conductor substrate, The process which embeds connection wiring in said 1st contact hole, and the process which forms a middle insulator layer on said 1st insulator layer so that connection wiring in said

1st contact hole may be covered, So that the process which forms the capacitor for charge storages equipped with the dielectric film inserted into the 1st electrode, 2nd electrode, and these electrodes on said middle insulator layer, and said capacitor for charge storages may be covered The process which forms the 2nd insulator layer on said middle insulator layer, and the process which forms the 2nd contact hole which etches said the 2nd insulator layer and said middle insulator layer, and results in connection wiring in said 1st contact hole, Connection wiring in the process which embeds connection wiring in said 2nd contact hole, and said 1st and 2nd contact holes is included. The process which forms wiring which connects electrically said drain or source, and said 1st electrode through said 1st contact hole and said 2nd contact hole is provided. Said middle insulator layer is the manufacture approach of the semiconductor memory characterized by consisting of a silicon nitride formed by the reduced pressure CVD method, and a silicon nitride formed by the plasma-CVD method.

[Translation done.]

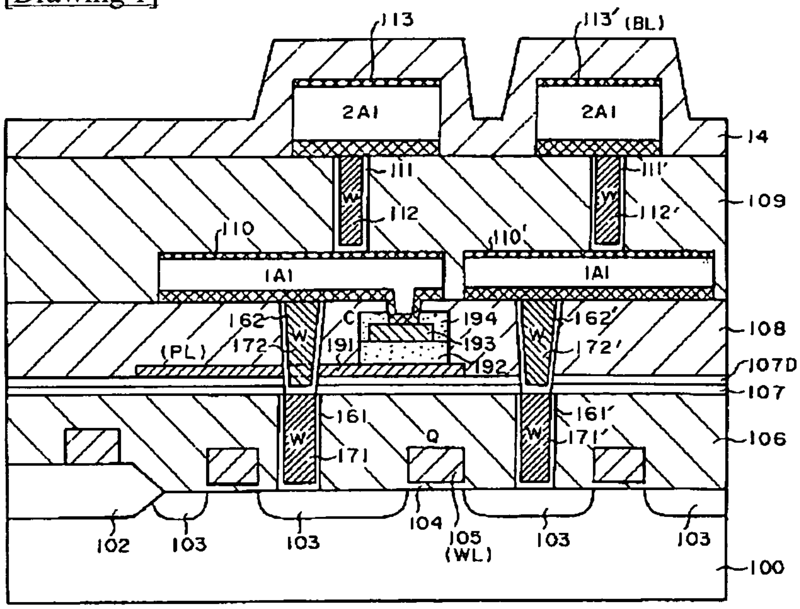
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view of the semiconductor memory of this invention.
[Drawing 2] The hysteresis characteristic Fig. showing the applied voltage / polarization property of the ferroelectric film.
[Drawing 3] The hysteresis characteristic Fig. of the condition which is not desirable as a FRAM cel.
[Drawing 4] The circuit diagram of the FRAM cel explaining write-in actuation of FRAM.
[Drawing 5] The potential variation diagram of the plate electrode PL at the time of the writing of a FRAM cel.
[Drawing 6] The expansion fragmentary sectional view of the semi-conductor substrate shown in drawing 1 .
[Drawing 7] The sectional view of the conventional semi-conductor substrate which compares drawing 6 .
[Drawing 8] The expanded sectional view of the capacitor shown in drawing 1 .
[Drawing 9] The top view of the capacitor shown in drawing 8 .
[Drawing 10] The sectional view of the semi-conductor substrate explaining the production process of the 2nd contact hole in the 1st example.
[Drawing 11] The sectional view of the semi-conductor substrate explaining the process which embeds connection wiring at the 1st contact hole of the 2nd example.
[Drawing 12] The sectional view of the conventional semiconductor memory.
[Description of Notations]
1,100,200 ... Semi-conductor substrate 2,102 ... Component isolation region, 3,103,203 ... Impurity diffusion field (the source / drain field), 4,104 ... Gate oxide 5,105 ... Gate electrode, 6,106,206 ... The 1st insulator layer (interlayer insulation film), 7,107 ... Middle insulator layer, 8,108 ... The 2nd insulator layer, 9,109 ... The 3rd insulator layer, 10, 10', 13, 13', 110, 110', 113, 113' ... Wiring, 11, 11', 111, 111' ... The 3rd contact hole, 12, 12', 71, 71', 72, 72', 112, 112', 171, 171', 172, 172', 271 ... 14 Connection wiring, 114 ... Protection insulator layer, 61, 61', 161, 161', 261 ... The 1st contact hole, 62, 62', 162, 162' ... The 2nd contact hole, 71A, 171A, 271A ... Tungsten (W) film, 71B, 171B, 271B ... A barrier metal layer, 91,191 ... Lower electrode 92,192 ... Ferroelectric film, 93,193 ... An up electrode, 107A, 107C ... The silicon nitride formed by the reduced pressure CVD method, 107B ... The silicon nitride, 107D which were formed by the plasma-CVD method ... A middle insulator layer (TEOS film by the reduced pressure CVD method), 191 A...Pt film 191 B...Ti film 194 ... Protective coat.

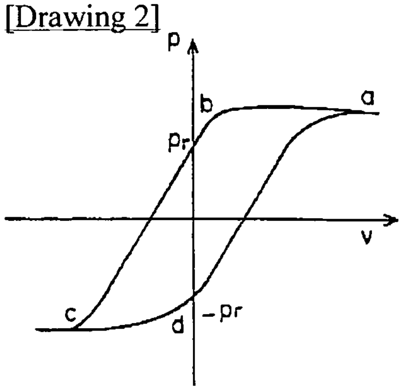
[Translation done.]

DRAWINGS

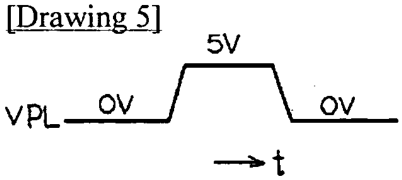
[Drawing 1]



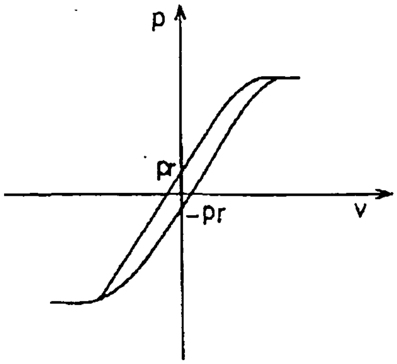
[Drawing 2]



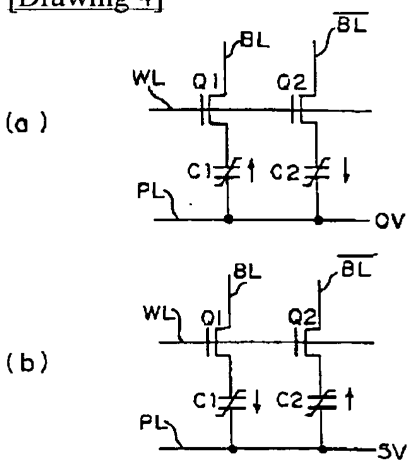
[Drawing 5]



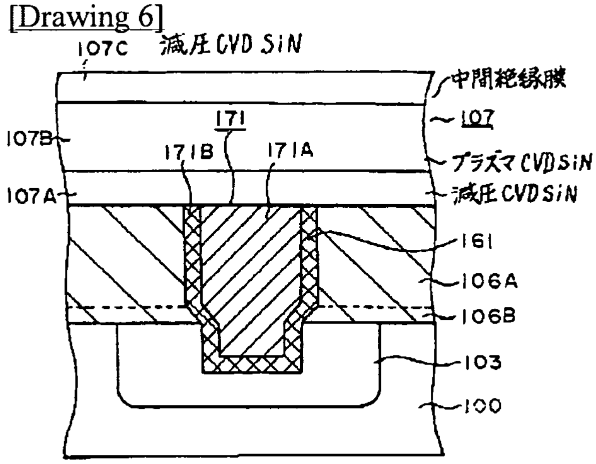
[Drawing 3]



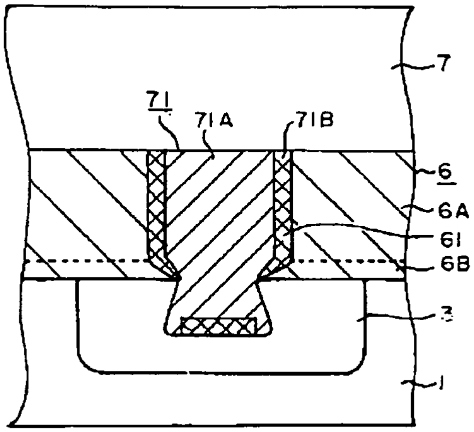
[Drawing 4]



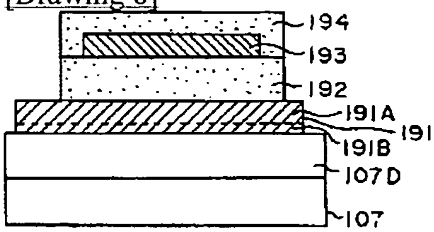
[Drawing 6]



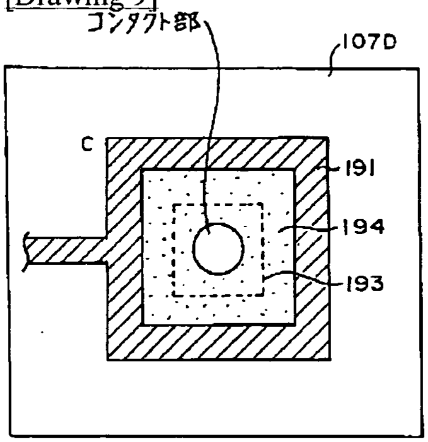
[Drawing 7]



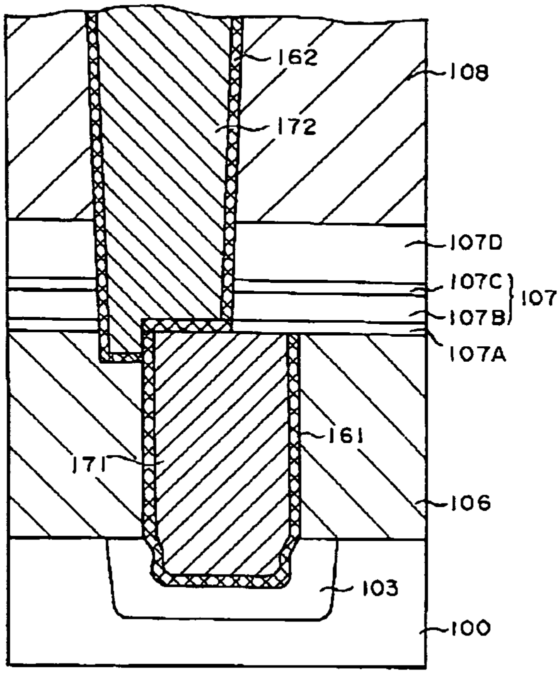
[Drawing 8]



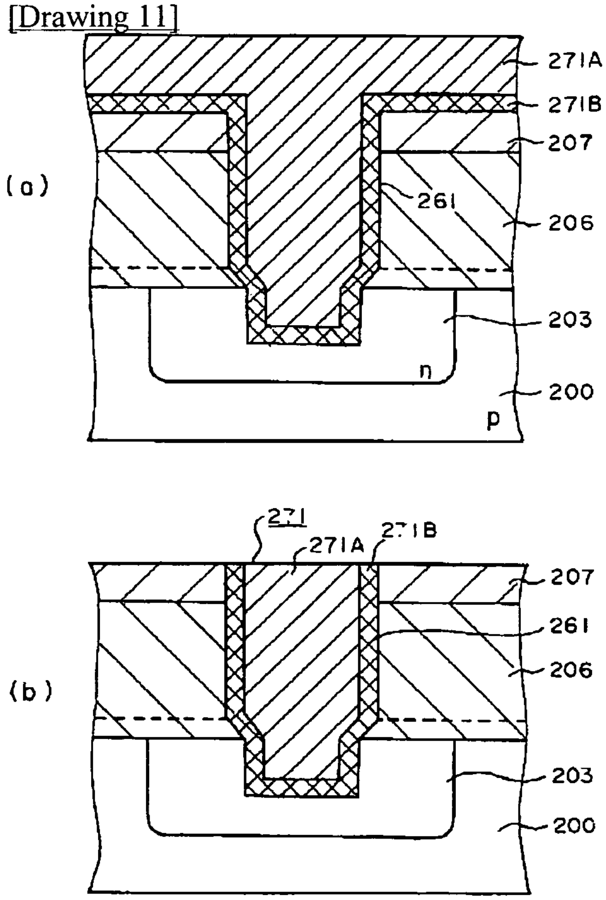
[Drawing 9]



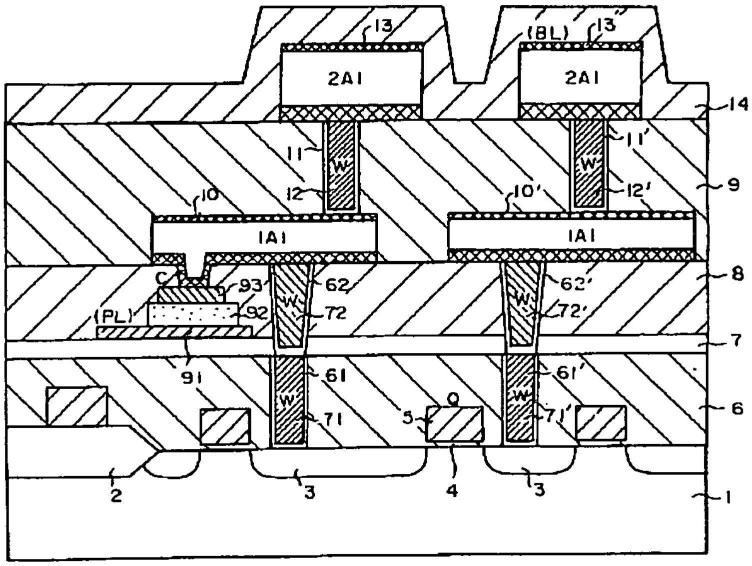
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]